L Number	Hits	Search Text	DB	Time stamp
1	0	(VERILOG or VHDL) and (DUT or (Device adj under adj test)) and ((clock adj credit) or (clock adj token))	USPAT	2004/01/13 13:44
2	106	(VERILOG or VHDL) and (DUT or (Device adj under adj test))	USPAT	2004/01/13 13:14
3	1	((VERILOG or VHDL) and (DUT or (Device adj under adj test))) and (clock same token)	USPAT	2004/01/13 13:16
4	0	((VERILOG or VHDL) and (DUT or (Device adj under adj test))) and (clock same credit)	USPAT	2004/01/13 13:17
5	0	((VERILOG or VHDL) and (DUT or (Device adj under adj test))) and (clock same domain)	USPAT	2004/01/13 13:17
6	12	((VERILOG or VHDL) and (DUT or (Device adj under adj test))) and clock and domain	USPAT	2004/01/13 13:44
7	2050	VERILOG or VHDL	USPAT	2004/01/13 13:44
8	95	(VERILOG or VHDL) and (clock same domain)	USPAT	2004/01/13 13:45
9	0	((VERILOG or VHDL) and (clock same domain)) and (clock same credit)	USPAT	2004/01/13 13:45
10	0	((VERILOG or VHDL) and (clock same domain)) and credit	USPAT	2004/01/13 13:45
11	11	((VERILOG or VHDL) and (clock same domain)) and token	USPAT	2004/01/13 14:07
12	5	clock.ti. and simulation.ti.	USPAT	2004/01/13 14:10
13	13	simulat$4.ti. and module$1.ti.	USPAT	2004/01/13 14:22
14	311	simulat$4 adj module$1	USPAT	2004/01/13 14:22
15	7	(simulat$4 adj module$1) and (clock same domain)	USPAT	2004/01/13 14:23